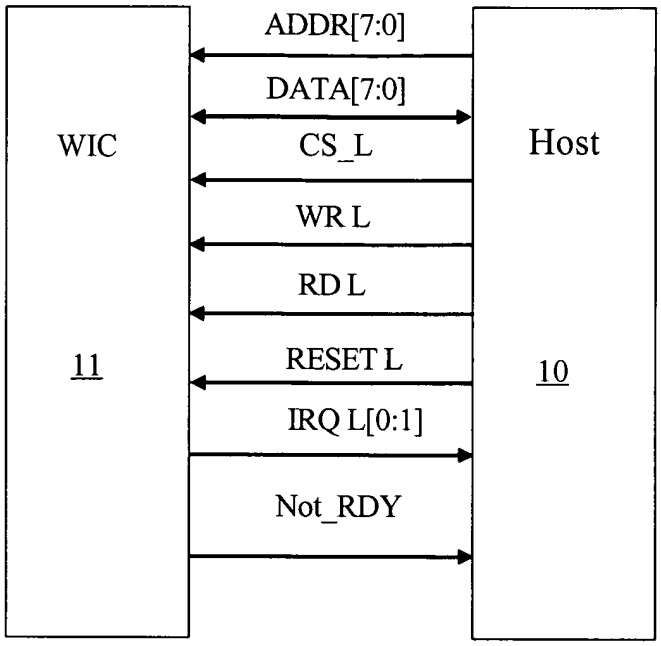

PRIOR ART

Fig. 1

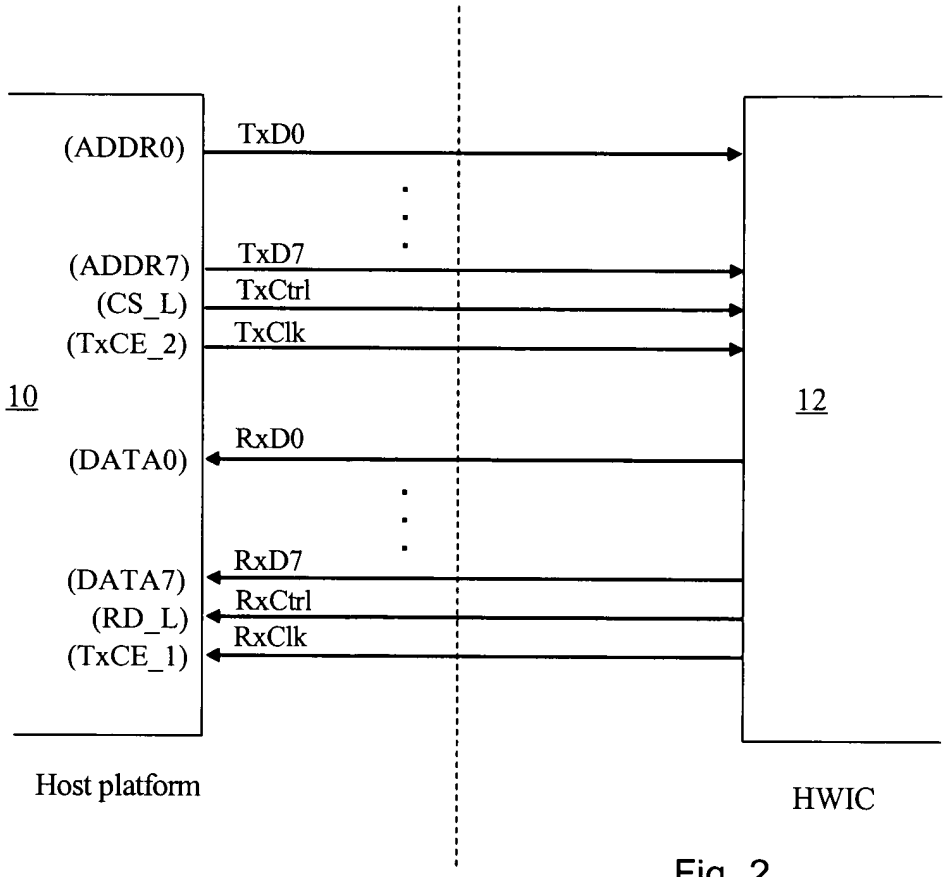

Fig. 2

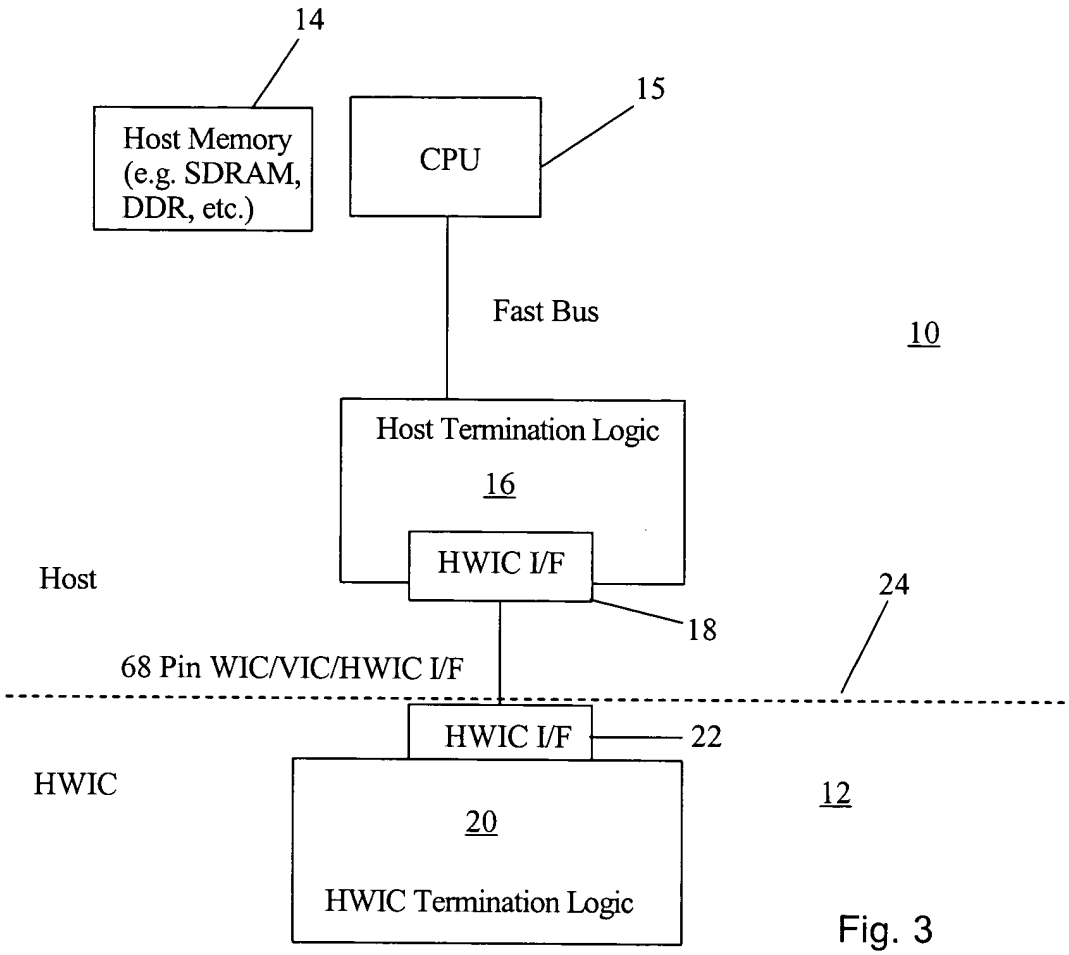
14
Host Memory (e.g. SDRAM, DDR, etc.)
15
CPU
Fast Bus
10
Host Termination Logic
16
HWIC I/F
18
Host
24
68 Pin WIC/VIC/HWIC I/F
HWIC I/F
22
HWIC
12
20
HWIC Termination Logic

Fig. 3

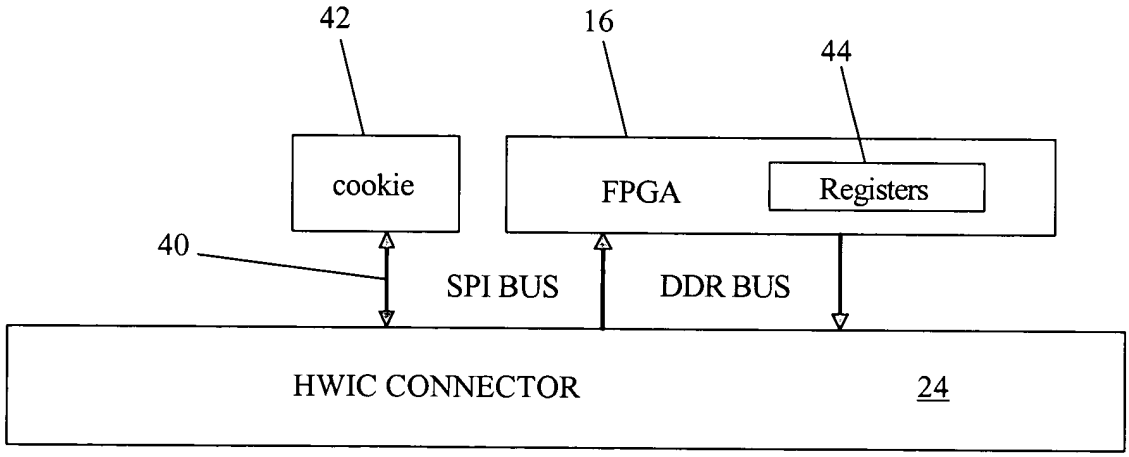
42
16
44
cookie
FPGA
Registers
40
SPI BUS
DDR BUS
HWIC CONNECTOR
24

Fig. 4

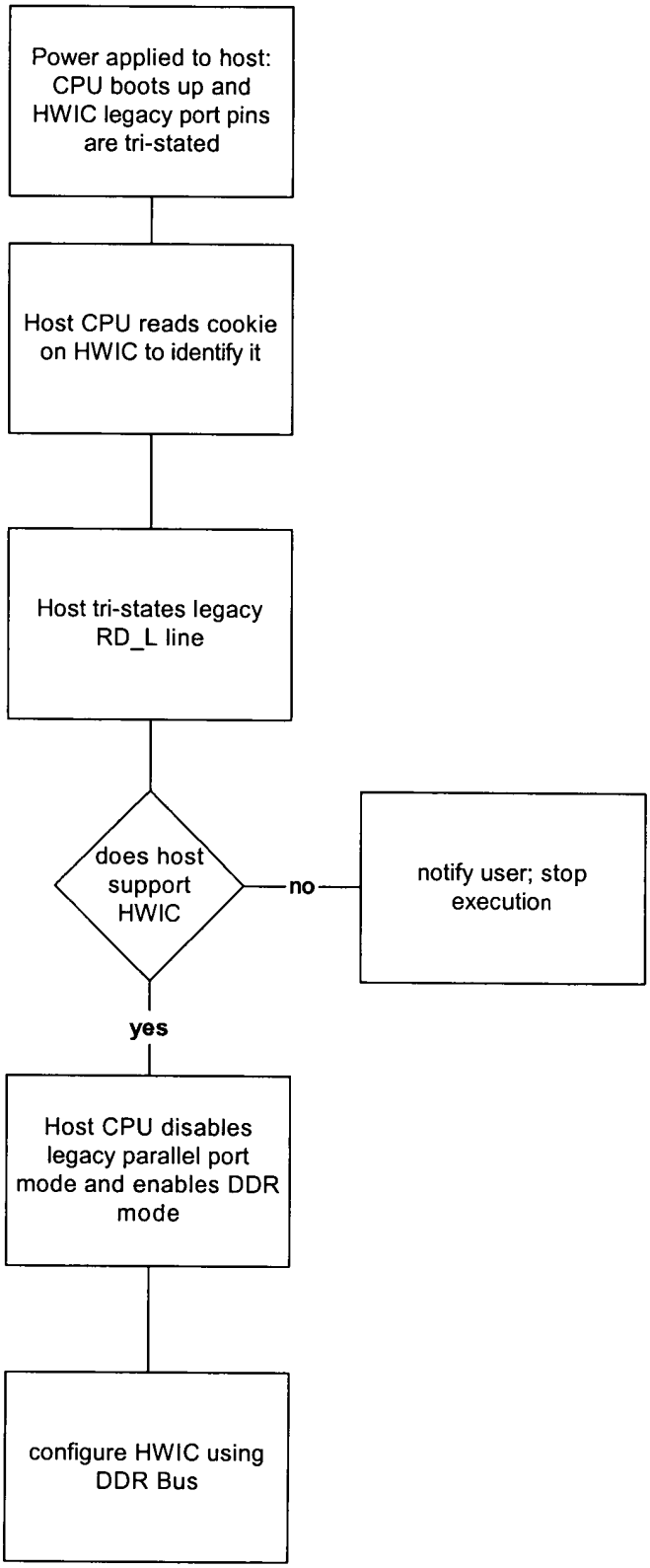
Power applied to host: CPU boots up and HWIC legacy port pins are tri-stated
Host CPU reads cookie on HWIC to identify it
Host tri-states legacy RD_L line
does host support HWIC
no
notify user; stop execution
yes
Host CPU disables legacy parallel port mode and enables DDR mode
configure HWIC using DDR Bus

Fig. 5

Command Opcode	Address	CRC8
0x01	32 Bits	8 bits

Fig. 6A

Command Opcode	Address	Data	CRC8
0x02	32 Bits	8 bits	8 bits

Fig. 6B

Command Opcode	Address	Data	CRC8
0x08	32 Bits	8 bits	8 bits

Fig. 7A

Command Opcode
0x1F

Fig. 7B

Command Opcode	Source	CRC8
0x0C	16 bits	8 bits

Fig. 8

Command Opcode	Data	*(Optional)* Rx Flags	CRC8
0x11	N bytes	8 bits	8 bits

Fig. 9

DMA Read Opcode	Address	Length	CRC8
0x61	32 bits	16 bits	8 bits

Fig. 10

DMA Read Response Opcode	Address	Length	Header CRC8	Data	Frame CRC8
0x62	32 bits	16 bits	8 bits	"Length" bytes	8 bits

Fig. 11

DMA Write Opcode	Address	Length	Header CRC8	Data	Frame CRC8
0x66 or 0x67	32 bits	16 bits	8 bits	"Length" bytes	8 bits

Fig. 12